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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,782	10/21/2003	Jin-Hyuk Lee	9903-071	5611

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,782	LEE ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7,9,10 and 12-21* is/are pending in the application.

4a) Of the above claim(s) *13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7,9,10,12 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2-22-6 has been entered.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3, 4, 7, 10, 12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (6780748) and Cho (6400021).

At column 7, lines 13-24 and column 11, line 35 to column 12, line 5, Yamaguchi discloses the following:

A method for a wafer level chip scale package (CSP), the method comprising: providing a semiconductor wafer 10, the semiconductor wafer including semiconductor chips 11 having chip pads 1 and a passivation layer 22a, the wafer further including scribe lines (illustrated in FIG. 5 (a), not labeled) between the chips; forming a first patterned dielectric layer 22b on the passivation layer that exposes the chip pads; forming a second patterned dielectric layer 25 on the first patterned dielectric layer that exposes the chip pads; forming a portion on the second patterned dielectric layer (abutting ball pad 2) where a ball pad 2 is to be formed; forming a metal wiring layer 3 on the first and second patterned dielectric layers including the portion, the metal wiring layer being electrically connected to the chip pads; forming a third dielectric layer 26 on the metal wiring layer; and removing a portion of the third dielectric layer over the portion to form a connection hole "areas above the bump pads 2" therein, the connection hole

exposing a portion of the metal wiring layer to form the ball pad; forming a solder ball 12 on the ball pad; and cutting the semiconductor wafer along the scribe lines "dicing."

A method for a wafer level chip scale package (CSP) comprising: providing a semiconductor wafer, the semiconductor wafer including semiconductor chips each having chip pads and a passivation layer; forming a first dielectric layer on the passivation layer; patterning the first dielectric layer to expose the chip pads; forming a second dielectric layer on the patterned first dielectric layer; patterning the second dielectric layer to expose the chip pads; forming a portion on the second patterned dielectric layer; forming a metal wiring layer on the first and second patterned dielectric layers, the metal wiring layer being electrically connected to the chip pads; forming a third dielectric layer on the metal wiring layer; and removing a portion of the third dielectric layer to form a connection hole therein, the connection hole exposing a portion of the metal wiring layer over the portion on the second patterned dielectric layer to form a ball pad; forming a solder ball on the ball pad.

A method of making a wafer level chip scale package (CSP), the method comprising: providing a semiconductor wafer, the semiconductor wafer including a semiconductor chip having chip pads and a passivation layer, the wafer further including scribe lines between the chips; forming a

first patterned dielectric layer on the passivation layer that exposes the chip pads; forming a second patterned dielectric layer on the first patterned dielectric layer that exposes the chip pads, wherein the first and second patterned dielectric layers have a portion where a ball pad is to be formed; forming a metal wiring layer on the first and second patterned dielectric lavers the metal wiring layer being electrically connected to the chip pads: forming a third dielectric laver on the metal wiring layer; and removing a portion of the third dielectric laver to form a connection hole that exposes a portion of the metal wiring layer.

However, Yamaguchi does not appear to explicitly disclose forming an embossed portion on the second patterned dielectric layer, including a concave portion that exposes a portion of the first patterned dielectric layer where a ball pad is to be formed and a convex portion that is formed from the second patterned dielectric layer; an embossed portion on the second patterned dielectric layer; forming a concave portion in the embossed portion that includes an exposed portion of the first dielectric layer where a ball pad is to be formed; forming a convex portion in the embossed portion of the second dielectric layer; a portion comprising an annular concave portion and an annular convex portion, the concave portion exposing a portion of the first patterned dielectric layer where a ball pad is to be formed, the convex portion being formed of the second dielectric layer;

wherein the convex portion is contained within the concave portion; wherein the convex portion is bounded by substantially vertical side walls and wherein said method further includes forming a ball pad on the concave portion, the convex portion, and the walls.

Nonetheless, at column 4, lines 13-18; column 4, line 57 to column 5, line 4; and column 5, lines 54-59, Cho discloses forming an embossed portion 30, 32 on the second patterned dielectric layer 30, including a concave portion 32 that exposes a portion of the first patterned dielectric layer 20 where a ball pad 51 is to be formed and a convex portion (defined by 32, illustrated in Fig. 6, not labeled) that is formed from the second patterned dielectric layer; an embossed portion on the second patterned dielectric layer; forming a concave portion in the embossed portion that includes an exposed portion of the first dielectric layer where a ball pad is to be formed; forming a convex portion in the embossed portion of the second dielectric layer; a portion comprising an annular concave portion and an annular convex portion, the concave portion exposing a portion of the first patterned dielectric layer where a ball pad is to be formed, the convex portion being formed of the second dielectric layer; wherein the convex portion is contained within the concave portion; wherein the convex portion is bounded by substantially vertical side walls and wherein said method further includes forming a ball pad on the concave portion, the convex

portion, and the walls. Moreover, it would have been obvious to combine this disclosure of Cho with the disclosure of Yamaguchi because it would strengthen the adhesion force between the solder ball 12 and pad 2.

Also, Yamaguchi and Cho do not appear to explicitly disclose wherein the concave portion comprises a circle shape, and the convex portion has an annular shape; wherein the convex portion comprises a discontinuous ring shape; and an annular concave portion.

Nonetheless, as reasoned from well established legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that, in view of the applied prior art, the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. For that matter, applicant has not disclosed that the dimensions are for **any** purpose or produce **any** result. Moreover, it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC

Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 3, 4, 5, 9, 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi and Cho as applied to claims 3 and 17 supra, and further in combination with Peng (6444295).

Yamaguchi and Cho do not appear to explicitly disclose wherein the concave portion comprises a circle shape, and the convex portion has an annular shape; wherein the convex portion comprises a discontinuous ring shape; wherein an area of the concave portion is inside the convex portion; wherein forming a second patterned dielectric layer comprises exposing a portion of the first patterned dielectric layer inside the annular convex portion; and an annular concave portion.

Still, as elucidated supra, Yamaguchi and Cho discloses exposing the first patterned dielectric inside the portion on the second patterned dielectric area. Further, at column 3, lines 19-47; and column 4, lines 11-13, Peng discloses wherein the concave portion (of 320, illustrated in FIG.2(a), not labeled) comprises a circle shape "ring," and the convex portion (of 320, illustrated in FIG.2(a), not labeled) has an annular shape; wherein the convex portion comprises a discontinuous ring shape (each concentric ring is discontinuous with another ring); wherein an area of the concave portion is

inside the convex portion; and an annular concave portion. In addition, the combination of Yamaguchi and Peng would result in the process wherein forming a second patterned dielectric layer comprises exposing a portion of the first patterned dielectric layer inside the annular convex portion. Moreover, it would have been obvious to combine this disclosure of Peng with the disclosure of the combination of Yamaguchi and Cho because it would facilitate the provision of the concave and convex portions of Yamaguchi and Cho and increase the firmness of the ball bond.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi and Cho as applied to claim 19 supra, and further in combination with Yunus (20030234447).

Yamaguchi and Cho do not appear to explicitly disclose wherein the convex portion comprises a plurality of arcuate portions, each having substantially vertical end walls and wherein the ball pad is also formed on the end walls.

Nevertheless, at paragraph 57, Yunus discloses wherein the convex portion 904 comprises a plurality of arcuate portions 904, each having substantially vertical end walls and wherein the ball pad 904 is also formed on the end walls. Furthermore, it would have been obvious to combine this disclosure of Yunus with the disclosure of Yamaguchi and Cho because it would enable gas venting during solder reflow of the ball of Yamaguchi.

Applicant's remarks filed 2-22-6 have been fully considered and are adequately addressed by the rejections supra.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
8-Jun-06